UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,056	05/20/2004	Ryosuke Inagaki	KY-202	6741

7590 01/09/2008

MATTINGLY, STANGER & MALUR, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
SUTHERS, DOUGLAS JOHN	

ART UNIT	PAPER NUMBER
2615	

MAIL DATE	DELIVERY MODE
01/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,056	INAGAKI, RYOSUKE	
	Examiner	Art Unit	
	Douglas Suthers	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 12/18/07 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-5, and 9-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 3 and 8, the claims recite "less than a few tens m sec. ". It is unclear what unit of time this represents. It is suggested to completely write out the time such as "milliseconds".

Regarding claims 4 and 9, it is unclear how the switch can be made up of transistors of the output stage, and be between the output stage and speaker as required by claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heithoff (US 6346854 B1) in view of Ishida (US 2002/0075072 A1).

Regarding claim 1, Heithoff discloses a mute circuit in a BTL circuit formed in an IC which drives a speaker (figure 2, 114) by a first output stage amplifier (116) and a second output stage amplifier (124) which generates an inverted output signal with respect to an output signal of the first output stage amplifier, wherein the second output stage amplifier receives the output signal of the first output stage amplifier as an input and generates the inverted output signal, a switch circuit (142) is provided and through a mute signal (CSD) the switch circuit is turned OFF to effect muting.

Heithoff does not expressly disclose the claimed switching position.

Ishida discloses wherein a switch circuit is provided between any one of the outputs of a first and second output stage amplifier (figure 1, items 5 and 9) and a terminal of the speaker and through a mute signal (12) the switch circuit is turned OFF for a predetermined interval to effect muting (paragraph [0012]).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the switching of Ishida in the system of Heithoff. The motivation for doing so would have been cut off current to the speaker from the power amps in a more direct manner, insuring no sound is heard. Therefore, it would have been obvious to combine Ishida with Heithoff to obtain the invention as specified in claim 1.

Regarding claim 2, Heithoff discloses wherein the second output stage amplifier receives the output signal of the first output stage amplifier via a resistor (R12).

Ishida discloses further comprising a mute signal generation circuit (described in [0012]) for generating the mute signal, the switch circuit is an analog switch (paragraph [0014]) and the mute signal is a pulse signal having a predetermined width which is generated when a power source is turned ON or OFF (required from item 12 figure 2, to items 5 and 9 according to paragraph [0012]).

Regarding claim 6, Heithoff discloses a BTL audio amplifier apparatus formed in an IC which drives a speaker (figure 2, item 114) by a first output stage amplifier (116) and a second output stage amplifier (124) which generates an inverted output signal with respect to an output signal of the first output stage amplifier, wherein the second

output stage amplifier receives the output signal of the first output stage amplifier as an input and generates the inverted output signal, a first switch circuit is provided (142) and through a mute signal (CSD) the first switch circuit is turned OFF to effect muting.

Heithoff does not expressly disclose the claimed switching position.

Ishida discloses wherein a first switch circuit is provided between any one of the outputs of the first and second output stage amplifier and a terminal of the speaker (figure 1, items 5 and 9) and through a mute signal (12) the first switch circuit is turned OFF for a predetermined interval to effect muting (paragraph [0012]).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the switching of Ishida in the system of Heithoff. The motivation for doing so would have been cut off current to the speaker from the power amps in a more direct manner, insuring no sound is heard. Therefore, it would have been obvious to combine Ishida with Heithoff to obtain the invention as specified in claim 6.

Regarding claim 7, Heithoff discloses wherein the second output stage amplifier receives the output signal of the first output stage amplifier via a resistor (R12).

Ishida discloses further comprising a mute signal generation circuit for generating the mute signal (described in [0012]), the first switch circuit is an analog switch (paragraph [0014]) and the mute signal is a pulse signal having a predetermined width which is generated when a power source is turned ON or OFF (required from item 12 figure 2, to items 5 and 9 according to paragraph [0012]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas Suthers whose telephone number is (571)272-0563. The examiner can normally be reached on 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571)272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

djs

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600